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EXAMINER	
GUARINO, RAHEL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/590,558	GAO ET AL.	
	Examiner	Art Unit	
	RAHEL GUARINO	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1, 23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to **non-statutory subject matter**.

Claim 1 pertains solely to a generation of an error signal and is directed to a judicial exception to 35 U.S.C. 101 (i.e., an abstract idea, natural phenomenon, or law of nature) and is not directed to a practical application of such judicial exception (e.g., because the claim does not require any physical transformation and the invention as claimed does not produce a useful, concrete, and tangible result).

Claims **2-11** are rejected as being dependent on rejected base claims.

Claim 23 pertains solely to a generation of an error signal for a delay-lock code tracking loop and is directed to a judicial exception to 35 U.S.C. 101 (i.e., an abstract idea, natural phenomenon, or law of nature) and is not directed to a practical application of such judicial exception (e.g., because the claim does not require any physical

transformation and the invention as claimed does not produce a useful, concrete, and tangible result).

Claims **24-34** are rejected as being dependent on rejected base claims.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims **23,35,43,51 are** rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification as original filed does not teach "method and apparatus for generating *a loop error signal for a delay-lock code tracking loop in a CDMA system".*

For the purpose of examination, examiner assumes to mean a process of locking the phase to the incoming signal according to the despread signal, According to the background (para#4).

Claims **24-34, 36-42, 44-50, 52-58** are rejected as being dependent on rejected base claims (**23, 35, 43, and 51**).

4. Claims **24-26, 36-38, 46-48, 54-56** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claims 24,36,46,54: the specification as originally filed failed to disclose "*calculating a first integral corresponding to products of some of the samples and a scrambling code sequence; calculating a second integral corresponding to products of later occurring ones of the samples and the scrambling code; and subtracting the second integral from the first integral to obtain the sign information*"

Re claims 26,38,48,56: The specification as originally filed failed to disclose "*wherein said accumulating step accumulates the sign information from a sample error signal e[m], wherein e[m] is equal to* $\sum_{n=0} N_0^{D-1} R_E [mN_D + n]Sc [mN_D + n] - \sum_{n=0} N^{D-1} R_L [mN_D + n] Sc [mN_D + n]$ *wherein* R_E *and* R_L *respectively represent earlier occurring samples and later occurring samples with respect to*

on-time occurring samples, n is an index of the samples in a chip rate, N_D is a code tracking dwell time, Sc is a local scrambling code sequence, and m is an index of the sample error signal e[m]"

Claims **25, 37, 47, 55** are rejected as being dependent on rejected base claims (**24, 36, 46, and 54**).

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims **8,12,20,30,43,50,51 are** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **Claim 8** recites the limitation "the step of utilizing values of the error signal" in page 4 line 9.

There is insufficient antecedent basis for this limitation in the claim.

8. **Claim 12** cites "decimating the accumulated sign information". It is unclear how to decimate the accumulated sign information since the sign information is a value of (+1 or -1).

9. **Claim 20** cites “decimating the accumulated sign information”. It is unclear how to decimate the accumulated sign information since the sign information is a value of (+1 or -1).

10. **Claim 30** recites the limitation "said of adjusting step" in page 8 line 5.

There is insufficient antecedent basis for this limitation in the claim.

11. **Claim 43** cites “decimating the accumulated sign information”. It is unclear how to decimate the accumulated sign information since the sign information is a value (+1 or -1).

12. **Claim 50** recites the limitation "said of adjusting step" in page 11 line 14.

There is insufficient antecedent basis for this limitation in the claim.

13. **Claim 51** cites “decimating the accumulated sign information”. It is unclear how to decimate the accumulated sign information since the sign information is a value (+1 or -1).

Claims **15, 16, 21, 22, 44, 45, 52, 53** are rejected as being dependent on rejected base claims (**12, 20, 43, and 51**).

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1,5,6,11,17,18 are rejected under 35 U.S.C. 102(b) as being anticipated by Gregorian et al. US 2002/0067788

Re claim 1, Gregorian discloses a method for generating an error signal, comprising the steps of (*fig.1*);

accumulating sign information *(+1,-1; accumulator (20))* relating to phase differences in received signals (*para#14*);

comparing (*comparator 32*) the accumulated sign information against predetermined threshold levels (*para#15; maximum and minimum threshold*);

generating the error signal when at least one of the predetermined threshold levels is satisfied (*para#16).*

Re claim 5, the method of claim 1, wherein said predetermined threshold levels include a positive threshold and a negative threshold *(+/-7 bits resolution, para#15*).

Re claim 6, the method according to claim 5, wherein said generating step comprises the steps of generating a positive constant error signal (*advanced signal*) when the positive threshold (*maximum*) is satisfied (*para#16 lines 1-3*), and generating a negative constant error (*delayed signal*) signal when the negative threshold level

(*minimum*) is satisfied (*para#16 lines 4-6*).

Re claim 11, the method of claim 1, further comprising the step of resetting (*reset, OR gate*) the accumulated sign information when the error signal is generated (*para#17*).

Re claim 17, Gregorian discloses an apparatus for generating an error signal, comprising the steps of (*fig.1);*

accumulating sign information *(+1,-1; accumulator (20))* relating to phase differences in received signals (*para#14*);

comparing (*comparator 32*) the accumulated sign information against predetermined threshold levels (*para#15; maximum and minimum threshold*);

the error signal generator for generating when at least one of the predetermined threshold levels is satisfied (*para#16*).

Re claim 18, the apparatus according to claim 17, wherein said generating step comprises the steps of generating a positive constant error signal (*advanced signal*) when the positive threshold (*maximum*) is satisfied (*para#16 lines 1-3*), and generating a negative constant error (*delayed signal*) signal when the negative threshold level (*minimum*) is satisfied (*para#16 lines 4-6*).

16. **Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorian et al. US 2002/0067788 in view of Kenney et al. US 6,741,665**

Re claim 2, the method of claim 1 does not teach wherein the error signal is generated in an automatic frequency control (AFC) loop in a Code Division Multiple Access (CDMA) system.

However, Kenney teaches wherein the error signal is generated in an automatic frequency control (AFC) loop (fig.1A) in a Code Division Multiple Access (CDMA) system (*col. 1 lines 25-30*).

Therefore, taking the combined teaching of Gregorian and Kenney as a whole would have been rendered obvious to one skilled in the art to modify Gregorian to utilize the error signal generated in an automatic frequency control (AFC) loop in a Code Division Multiple Access (CDMA) system for the benefit of allowing more robust automatic frequency control (AFC) loop circuitry (col. 6 lines 33-38, Kenney).

17. **Claims 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorian et al. US 2002/0067788 in view of Kenney et al. US 6,741,665 in further view of Ling et al. US 6,363,102**

Re claim 3, the modified invention as claimed in claim 2 does not teach multiplying a current despread pilot signal with a complex conjugate of a previous despread pilot signal; and obtaining a sign value of a product of said multiplying step.

However, Ling discloses multiplying a current despread pilot signal with a complex conjugate of a previous despread pilot signal (*col. 3 lines 6-9*); and obtaining a sign value of (*f^)* a product of said multiplying step (*col. 3 lines 6-12*).

Therefore, taking the combined teaching of Gregorian, Kenney and Ling as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Gregorian and Kenney to further generate current despread pilot signal with a complex conjugate of a previous despread pilot signal; and obtaining a sign value of a product according to Ling for the benefit of allowing adjusting the phase of the received data.

Re claim 4, the modified invention as claimed in claim 3, wherein said step of obtaining a sign value comprises the step of extracting the sign value of an imaginary (*Im*) part of the product of said multiplying step (*col. 3 lines 6-12; Ling*).

18. **Claims 7-9,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorian et al. US 2002/0067788 in view of Baum et al. US 5,740,205**

Re claim 7, the method according to claim 6 does not teach wherein the positive constant error signal and the negative constant error signal are used to control a gain of an AFC loop.

In the same field of endeavor, However, Baum discloses wherein the positive constant error signal and the negative constant error signal are used to control a gain (*k is the PLL loop gain of the AFC*) of an AFC loop (*col. 9 lines 64 to col. 10 lines 34*).

Therefore, taking the combined teaching of Gregorian and Baum as a whole would have been rendered obvious to one skilled in the art to modify Gregorian to utilize Baum's positive constant error signal and negative constant error signal to control the PLL loop gain of the AFC for the benefit of frequency offset correction of the automatic frequency loop (*col. 11 lines 66 to col. 12 lines 1*; *Baum*).

Re claim 8, the method according to claim 1 does not teach further comprising the step of utilizing values of the error signal to control a gain in an AFC loop.

In the same field of endeavor, However, Baum teaches utilizing values (*phase error values*) of the error signal to control a gain in an AFC loop (*col. 6 lines 33-39*).

Therefore, taking the combined teaching of Gregorian and Baum as a whole would have been rendered obvious to one skilled in the art to modify Gregorian to utilize Baum's values of the error signal to control a gain in an AFC loop for the benefit of correcting the frequency offset of the received signal (*col. 6 lines 59 to col. 7 lines 4; Baum)*.

Re claim 9, the modified invention as claimed in claim 8, wherein the values of the error signals are constant values *(+1,-1)* capable of being adjusted to control the gain in the AFC loop (*col. 6 lines 59 to col. 7 lines 4; Baum*).

Re claim 19, the apparatus according to claim 18 does not teach wherein the positive constant error signal and the negative constant error signal are used to control a gain of an AFC loop.

In the same field of endeavor, However, Baum discloses wherein the positive constant error signal and the negative constant error signal are used to control a gain (*k is the PLL loop gain of the AFC*) of an AFC loop (*col. 9 lines 64 to col. 10 lines 34*).

Therefore, taking the combined teaching of Gregorian and Baum as a whole would have been rendered obvious to one skilled in the art to modify Gregorian to utilize Baum's positive constant error signal and negative constant error signal to control the PLL loop gain of the AFC for the benefit of frequency offset correction of the automatic frequency loop (*col. 11 lines 66 to col. 12 lines 1*; *Baum*).

19. **Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gregorian et al. US 2002/0067788 in view of Hietala US 6,229,991**

Re claim 10, the method of claim 1 does not teach utilizing the predetermined threshold levels to affect a bandwidth of an AFC loop.

However, Hietala discloses utilizing the predetermined threshold levels (*abstract*).

Therefore, taking the combined teaching of Gregorian and Hietala as a whole would have been rendered obvious to one skilled in the art to modify Gregorian to utilize

the predetermined threshold levels to affect a bandwidth of an AFC loop for the benefit of enabling AFC synchronization (*col.5 lines 61-65, Hietala*).

20. Claims 12,15,16,20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenney et al. US 6,741,665 in view of Rouphael US 6,304,620

Re claim 12, Kenney discloses a method for generating an error signal for an automatic frequency control (AFC) loop (fig.1A) in a Code Division Multiple Access (CDMA) system (CDMA; col.1 lines 26-30), comprising the steps of:
accumulating sign information (*10*) relating to phase differences in received pilot signals *(col. 2 lines 7-10);* utilizing an output of the error signal for the AFC loop (col. *3 lines 46-50*);does not teach decimating the accumulated sign information and utilizing an output of said decimating step as the error signal.

However, Rouphael discloses decimating to a lower rate (*col. 5 lines 53-55);* and utilizing an output of said decimating step as the error signal (*col. 5 lines 55-59*)

Therefore, taking the combined teaching of Kenney and Rouphael as a whole would have been rendered obvious to one skilled in the art to modify Kenney to decimate to a lower rate and the error signal as taught by Rouphael for the benefit of improving the SNR by smoothing out the noise.

Re claim 15, the modified invention as claimed in claim 12, wherein the output of said decimating step is utilized as the loop error signal upon a decimation of a threshold

number of the samples (*col. 6 lines 54-56, Rouphael*).

Re claim 16, the modified invention as claimed in claim 15, further comprising the step of resetting the output of said decimating step at a same interval (*set to zero*) as when the output of said decimator is utilized as the error signal (*col. 6 lines 45-56, Rouphael*).

Re claim 20, Kenney discloses an apparatus for generating an error signal for an automatic frequency control (AFC) loop in a Code Division Multiple Access (CDMA) system (fig.1A), comprising:

an accumulator for accumulating sign information (*10*) relating to phase differences in received pilot signals (*col. 1 lines 2-10*); does not teach a decimator for decimating the accumulated sign information so as to output the error signal therefrom.

However, Rouphael discloses decimating to a lower rate (*col. 5 lines 53-55*); and utilizing an output of said decimating as the error signal therefrom(*col. 5 lines 55-59*)

Therefore, taking the combined teaching of Kenney and Rouphael as a whole would have been rendered obvious to one skilled in the art to modify Kenney to decimate to a lower rate, the error signal as taught by Rouphael for the benefit of improving the SNR by smoothing out the noise.

Re claim 21, the modified invention as claimed in claim 20, wherein the output of said decimator step is utilized as the loop error signal upon a decimation of a threshold number of the samples (*col. 6 lines 54-56, Rouphael*).

Re claim 22, the modified invention as claimed in claim 21, wherein the output of said decimator is reset at a same interval (set to zero) as when the output of said

decimator is utilized as the error signal (*col. 6 lines 45-56, Rouphael*).

21. **Claims 13,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenney et al. US 6,741,665 in view of Rouphael US 6,304,620 in further view of in further view of Ling et al. US 6,363,102**

Re claim 13, the modified invention as claimed in claim 12 does not teach multiplying a current despread pilot signal with a complex conjugate of a previous despread pilot signal; and obtaining a sign value of a product of said multiplying step.

However, Ling discloses multiplying a current despread pilot signal with a complex conjugate of a previous despread pilot signal (*col. 3 lines 6-9*); and obtaining a sign value of (f^) a product of said multiplying step (*col. 3 lines 6-12).*

Therefore, taking the combined teaching of Kenney, Rouphael and Ling as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Gregorian and Rouphael to generate current despread pilot signal with a complex conjugate of a previous despread pilot signal; and obtaining a sign value of a product as taught by Ling for the benefit of allowing adjusting the phase of the received data.

Re claim 14, the modified invention as claimed in claim 13, wherein said step of obtaining a sign value comprises the step of extracting the sign value of an imaginary (Im) part of the product of said multiplying step (*col. 3 lines 6-12; Ling*).

22. **Claims 23,27,28-31,35,39,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. US 7,715,463**

Re claim 23, Li discloses a method for generating a loop error signal for a delay-lock code tracking loop in a CDMA system (*fig.4*), comprising the steps of: accumulating sign (*64*) information (+, -) relating to phase differences between samples of a received code sequence (col*. 6 lines 41-42, where accumulator is defined in equation 10*); does not explicitly teach comparing the accumulated sign information against adaptable threshold levels; and generating the loop error signal when at least one of the adaptable threshold levels is satisfied.

Instead, Li discloses adjusting forward or backward according to early or late sample (*col. 6 lines 52-55)* and generating the loop error signal (*col. 6 16-20*).

Therefore, it would have been rendered obvious to one skilled in the art to adjust forward or backward according to early or late sample and to generate the loop error signal for the benefit of improving the performance of code-tracking loop (CTL) by eliminating interference between fingers (*col. 9 lines 16-19*).

Re claim 27, the method according to claim 23, wherein the adaptable threshold levels include a positive threshold (+1) and a negative threshold (-1) (*col. 6 lines 48-52*).

Re claim 28, the method according to claim 27, wherein said generating step comprises the step of generating a positive constant loop error signal when the positive threshold is satisfied (*col.5 lines 63-65*), and generating a negative constant loop error signal when the negative threshold level is satisfied (*col.5 lines 65-67*).

Re claim 29, the method according to claim 28, wherein the positive constant loop error signal and the negative constant loop error are used to control the gain in the delay-lock code tracking loop (*col. 10 lines 40-49*).

Re claim 30, the method according to claim 23, utilizing values of the loop error signal to control a gain in the delay-lock code tracking loop (*col. 10 lines 25-33*).

Re claim 31, the method according to claim 30,wherein the values of the loop error signal are constant values (*equation 19 and 20*) capable of being adjusted to control the gain in the delay-lock code tracking loop (*col. 10 lines 40-49*).

Re claim 35, Li discloses an apparatus for generating a loop error signal for a delay-lock code tracking loop in a CDMA system (fig.4), comprising:
accumulator (*64*) accumulating sign information (+, -) relating to phase differences between samples of a received code sequence (*col. 6 lines 41-42, where accumulator is defined in equation 10);* does not explicitly teach comparator the accumulated sign information against adaptable threshold levels; and g error signal generator when at least one of the adaptable threshold levels is satisfied.

Instead, Li discloses adjustor (*65*) for adjusting forward or backward according to early or late sample (*col. 6 lines 52-55)* and error generator (*59*) for generating the loop error signal (*col. 6 16-20*).

Therefore, it would have been rendered obvious to one skilled in the art to adjust forward or backward according to early or late sample and to generate the loop error signal for the benefit of improving the performance of code-tracking loop (CTL) by eliminating interference between fingers (*col. 9 lines 16-19*)

Re claim 39, the apparatus according to claim 35, wherein said generating step comprises the step of generating a positive constant loop error signal when the positive threshold is satisfied (*col.5 lines 63-65*), and generating a negative constant loop error signal when the negative threshold level is satisfied (*col.5 lines 65-67*).

Re claim 40, the apparatus according to claim 39, wherein the positive constant error signal and the negative constant error signal are for controlling a gain of the delay-lock code tracking loop (*col. 10 lines 25-33*).

23. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. US 7,715,463 in view of Bultan et al. US 7,010,020

Re claim 32, the method according to claim 23 does not teach the step of utilizing the adaptable threshold levels to affect a bandwidth of the delay-lock code tracking loop (*col.2 lines 1-6*).

In the same field of endeavor, however, Bultan discloses utilizing the adaptable threshold levels to affect a bandwidth of the delay-lock code tracking loop (*col.4 lines 44-50*).

Therefore, taking the combined teaching of Li and Bultan as a whole would have been rendered obvious to one skilled in the art to modify Li to further include Bultan's adaptive threshold levels to affect a bandwidth of the delay-lock code tracking loop for the benefit of determining the main characteristics of the loop (*col. 4 lines 53-65;Bultan*).

24. Claims 33,34,41,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. US 7,715,463 in view of Pietraski et al. US 7,724,817

Re claim 33, the method according to claim 23 does not teach wherein the delay-lock code tracking loop includes a receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal.

However, Pietraski discloses a receiver sample buffer (*214*) from which the samples of the received code sequence (*210*) may be retrieved with different delays (*col. 7 lines 44-46*), and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal (*col. 7 lines 50-55).*

Therefore, taking the combined teaching of Li and Pietraski as a whole would have been rendered obvious to one skilled in the art to modify Li to further include Pietraski's receiver's sample buffer from which the samples of the received code

sequence may be retrieved with different delays, adjusting a position of the samples in the receiver sample buffer based on the loop error signal for the benefit of adjusting the amount of the delay according to velocity (*col. 8 lines 11-17; Pietraski*).

Re claim 34, the modified invention as claimed in claim 33, further comprising the step of filtering the loop error signal (*FIR filter;12*) prior to said adjusting step *(col.3 lines 45-49; Pietraski*).

Re claim 41, the apparatus according to claim 35 does not teach wherein the delay-lock code tracking loop includes a receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal.

However, Pietraski discloses a receiver sample buffer (*214*) from which the samples of the received code sequence (*210*) may be retrieved with different delays (*col. 7 lines 44-46*), and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal (*col. 7 lines 50-55).*

Therefore, taking the combined teaching of Li and Pietraski as a whole would have been rendered obvious to one skilled in the art to modify Li to further include Pietraski's receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, adjusting a position of the samples in the receiver sample buffer based on the loop error signal for the benefit of adjusting the amount of the delay according to velocity (*col. 8 lines 11-17; Pietraski*).

Re claim 42, the modified invention as claimed in claim 41, further comprising the step of filtering the loop error signal (*FIR filter;12*) prior to said adjusting step (*col.3 lines 45-49; Pietraski).*

25. **Claims 43,44,51,52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. US 7,715,463 in view of Kang et al. US 6,370,133**

Re claim 43, Li discloses a method for generating a loop error signal for a delay-lock code tracking loop in a CDMA system (fig.4), comprising the steps of: accumulating sign (*64*) information (+, -) relating to phase differences between samples of a received code sequence (*col. 6 lines 41-42, where accumulator is defined in equation 10);* does not explicitly teach decimating the accumulated sign information; and utilizing an output of said decimating step as the loop error signal for the delay-lock code tracking loop.

In the same field of endeavor, however, Kang discloses (*fig.4*) decimating the accumulated sign information (*col. 7 lines 35-39*); and utilizing an output of said decimating step as the loop error signal for the delay-lock code tracking loop (*col. 8 lines 31-43).*

Therefore, taking the combined teaching of Li and Kang as a whole would have been rendered obvious to one skilled in the art to modify Li to further decimate the accumulated sign information and utilizing an output of said decimating step as the error

signal for the benefit of removing any offset from the receiver signal (*col. 7 lines 42-46; Kang).*

Re claim 44, the modified invention as claimed in claim 43, wherein the output of said decimator step is utilized as the loop error signal upon a decimation of a threshold number of the samples (*col. 8 lines 31-43, Kang*).

Re claim 51, Li discloses an apparatus for generating a loop error signal for a delay-lock code tracking loop in a CDMA system (*fig.4*), comprising:
accumulating sign (*64*) information (+, -) relating to phase differences between samples of a received code sequence (*col. 6 lines 41-42, where accumulator is defined in equation 10);* does not explicitly teach decimating the accumulated sign information; and utilizing an output of said decimating step as the loop error signal for the delay-lock code tracking loop.

In the same field of endeavor, however, Kang discloses (*fig.4)* decimating the accumulated sign information (*col. 7 lines 35-39*); and utilizing an output of said decimating step as the loop error signal for the delay-lock code tracking loop *(col. 8 lines 31-43).*

Therefore, taking the combined teaching of Li and Kang as a whole would have been rendered obvious to one skilled in the art to modify Li to further decimate the accumulated sign information and utilizing an output of said decimating step as the error signal for the benefit of removing any offset from the receiver signal (*col. 7 lines 42-46; Kang).*

Re claim 52, the modified invention as claimed in claim 51, wherein the output of said decimator step is utilized as the loop error signal upon a decimation of a threshold number of the samples (*col. 8 lines 31-43, Kang*).

26. **Claims 45,53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. US 7,715,463 in view of Kang et al. US 6,370,133 in further view of Rouphael US 6,304,620**

Re claim 45, the modified invention as claimed in claim 44 does not teach wherein the output of said decimator is reset at a same interval as when the output of said decimator is utilized as the error signal.

However, Rouphael decimator is reset at a same interval (*set to zero*) as when the output of said decimator is utilized as the error signal (*col. 6 lines 45-58*)

Therefore, taking the combined teaching of Li, Kang and Rouphael as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Li and Kang to further reset at a same interval as when the output of said decimator is utilized as the error signal for the benefit of eliminating unwanted frequency offset.

Re claim 53, the modified invention as claimed in claim 52 does not teach wherein the output of said decimator is reset at a same interval as when the output of said decimator is utilized as the error signal.

However, Rouphael decimator is reset at a same interval (*set to zero*) as when the output of said decimator is utilized as the error signal (*col. 6 lines 45-58*)

Therefore, taking the combined teaching of Li, Kang and Rouphael as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Li and Kang to further reset at a same interval as when the output of said decimator is utilized as the error signal for the benefit of eliminating unwanted frequency offset.

27. Claims 49,50,57,58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. US 7,715,463 in view of Kang et al. US 6,370,133 in further view of Pietraski et al. US 7,724,817

Re claim 49, the modified invention as claimed in claim 43 does not teach wherein the delay-lock code tracking loop includes a receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal.

However, Pietraski discloses a receiver sample buffer (*214*) from which the samples of the received code sequence (*210*) may be retrieved with different delays (*col. 7 lines 44-46*), and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal (*col. 7 lines 50-55)*

Therefore, taking the combined teaching of Li, Kang and Pietraski as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Li and Kang to further include Pietraski's receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, adjusting a position of the samples in the receiver sample buffer based on the loop error signal for the benefit of adjusting the amount of the delay according to velocity *(col. 8 lines 11-17; Pietraski).*

Re claim 50, the modified invention as claimed in claim 43 does not teach filtering the loop error signal prior to said adjusting step.

However, Pietraski discloses filtering the loop error signal (*FIR filter; 12*) prior to said adjusting step (*col.3 lines 45-49*).

Therefore, taking the combined teaching of Li, Kang and Pietraski as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Li and Kang to further include Pietraski's filter for the benefit of removing the error signal.

Re claim 57, the modified invention as claimed in claim 51 does not teach wherein the delay-lock code tracking loop includes a receiver sample buffer from which

the samples of the received code sequence may be retrieved with different delays, and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal.

However, Pietraski discloses a receiver sample buffer (*214*) from which the samples of the received code sequence (*210*) may be retrieved with different delays (*col. 7 lines 44-46*), and the method further comprises the step of adjusting a position of the samples in the receiver sample buffer based on the loop error signal *(col. 7 lines 50-55).*

Therefore, taking the combined teaching of Li, Kang and Pietraski as a whole would have been rendered obvious to one skilled in the art to modify the combined invention of Li and Kang to further include Pietraski's receiver sample buffer from which the samples of the received code sequence may be retrieved with different delays, adjusting a position of the samples in the receiver sample buffer based on the loop error signal for the benefit of adjusting the amount of the delay according to velocity *(col. 8 lines 11-17; Pietraski).*

Re claim 58, the modified invention as claimed in claim 57, filtering the loop error signal (*FIR filter; 12*) prior to said adjusting step (*col.3 lines 45-49; Pietraski*).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rahel Guarino whose telephone number is (571)270-1198. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Payne David can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Rahel Guarino/
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